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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,076	10/04/2005	Andrei Terechko	NL030344US1	8796

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
05/10/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

vera.kublanov@philips.com
debbie.henn@philips.com
marianne.fox@philips.com

Office Action Summary	Application No.	Applicant(s)
	10/552,076	TERECHKO, ANDREI
	Examiner	Art Unit
	KEITH VICARY	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/21/2011 has been entered.

2. Claims 1-8 are pending in this office action and presented for examination. Claims 1 and 5 are newly amended by amendment filed 3/25/2011.

Claim Objections

3. Claims 1-8 are objected to because of the following informalities. Appropriate correction is required.

4. In claim 1, line 7, "one or more pipeline register" should be "one or more pipeline registers".

   a. Claims 2-4 are objected to for failing to alleviate the objection to claim 1 above.

5. In claim 5, line 7, "one or more pipeline register" should be "one or more pipeline registers".

b. Claims 6-8 are objected to for failing to alleviate the objection to claim 5 above.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 3-4 and 7-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

8. Claim 3 recites the limitation "said clusters are connected to each other via a bus connection" in line 2. Claim 3 is dependent on claim 1, which recites the limitation "one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of clusters" in lines 7-8. However, the original disclosure does not support the concept of one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of clusters, in the embodiment wherein said clusters are connected to each other via a bus connection. For example, see Figure 4, which shows the distance between cluster A and cluster B to be the same as the distance between cluster B and C, yet there is no pipeline register between cluster A and cluster B and a pipeline register between cluster

B and C. Therefore, in the embodiment wherein said clusters are connected to each other via a bus connection, pipeline registers are not placed depending on the distance between respective ones of said plurality of clusters.

Additionally, the original disclosure does not appear to support the concept of *one or more* pipeline register between said clusters, in the embodiment wherein said clusters are connected to each other via a bus connection. For example, see Figures 2 and 4, which show particular clusters (e.g. Clusters A and B; and Clusters C and D) being connected without one or more pipeline register.

Additionally, the original disclosure does not appear to support the concept of one *or more* pipeline register between said clusters, in the embodiment wherein said clusters are connected to each other via a bus connection. For example, see Figures 2 and 4, which do not show multiple pipeline registers between any two clusters; the explanatory disclosure for Figures 2 and 4 likewise do not disclose of multiple pipeline registers between any two clusters.

c. Claim 4 is rejected for failing to alleviate the rejection of claim 3 above.

9. Claim 7 recites the limitation "said clusters are connected to each other via a bus connection" in lines 2-3. Claim 7 is dependent on claim 5, which recites the limitation "one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of clusters" in lines 7-8. However, the original disclosure does not support the concept of one or more pipeline register between said clusters, depending on the distance between respective ones of said plurality of

clusters, in the embodiment wherein said clusters are connected to each other via a bus connection. For example, see Figure 4, which shows the distance between cluster A and cluster B to be the same as the distance between cluster B and C, yet there is no pipeline register between cluster A and cluster B and a pipeline register between cluster B and C. Therefore, in the embodiment wherein said clusters are connected to each other via a bus connection, pipeline registers are not placed depending on the distance between respective ones of said plurality of clusters.

Additionally, the original disclosure does not appear to support the concept of *one or more* pipeline register between said clusters, in the embodiment wherein said clusters are connected to each other via a bus connection. For example, see Figures 2 and 4, which show particular clusters (e.g. Clusters A and B; and Clusters C and D) being connected without one or more pipeline register.

Additionally, the original disclosure does not appear to support the concept of one *or more* pipeline register between said clusters, in the embodiment wherein said clusters are connected to each other via a bus connection. For example, see Figures 2 and 4, which do not show multiple pipeline registers between any two clusters; the explanatory disclosure for Figures 2 and 4 likewise do not disclose of multiple pipeline registers between any two clusters.

d. Claim 8 is rejected for failing to alleviate the rejection of claim 7 above.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

12. Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108) each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108), and a connection between respective ones of said plurality of clusters (Figure 12, which shows the clusters connected to each other via connections denoted by letters I-R).

However, Batten does not disclose of one or more pipeline registers in a connection depending on the distance between respective ones of said plurality of clusters, and one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster.

On the other hand, Nickolls does disclose of one or more pipeline registers in a connection depending on the distance between respective ones of said plurality of clusters, and control connections having a pipeline register, and one or more additional pipeline registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 20, lines 11-15, discloses of pipeline registers in the paths connecting different processing elements; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

13. Consider claim 2, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

14. Consider claim 3, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

15. Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (Figure 12, processor 100, comprised of clusters 108; the ILP aspect of the processor is conveyed in, for example, col. 7, lines 13-15, which discloses of multi-issue and VLIW embodiments), comprising a plurality of clusters (Figure 12, clusters 108) each comprising at least one register file (col. 3, line 66, remote clusters' register files) and at least one functional unit (col. 11, lines 7-8, each cluster contains four ALUs); an instruction unit for issuing control signals to said clusters (Figure 12, decode unit 106, shown sending control signals D-H to each cluster 108; col. 11, line 65 discloses these are instruction paths), wherein said instruction unit is connected to each of said clusters via respective control connections (Figure 12, paths D-H which connected the decode unit 106 to each cluster 108), and a connection between respective ones of said

plurality of clusters (Figure 12, which shows the clusters connected to each other via connections denoted by letters I-R).

However, Batten does not disclose of one or more pipeline registers in a connection depending on the distance between respective ones of said plurality of clusters, and one or more pipeline additional registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster.

On the other hand, Nickolls does disclose of one or more pipeline registers in a connection depending on the distance between respective ones of said plurality of clusters, and control connections having a pipeline register, and each control connection having a pipeline register, and one or more pipeline additional registers arranged in said control connections to a remote cluster of said plurality of clusters, depending on the distance between said instruction unit and said plurality of clusters, so as to pipeline said control connections to said remote cluster (col. 6, lines 11-14, partitioning a message routing path spatially into fractional segments and providing pipeline registers at the junctures of the segments for temporarily storing the bits of a transmitted message; col. 20, lines 11-15, discloses of pipeline registers in the paths connecting different processing elements; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires).

The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

16. Consider claim 6, Batten discloses said clusters are connected to each other via a point-to-point connection (Figure 12, which shows each cluster connected to each other cluster via one of paths I-R).

17. Consider claim 7, Batten discloses that said clusters are connected to each other via a bus connection (col. 9, line 66, set of busses).

18. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claims 3 and 7 above, and further in view of Pechanek et al. (Pechanek) (US 5659785).

19. Consider claim 4, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

20. Consider claim 8, Batten and Nickolls do not explicitly disclose that said control connections are implemented as a bus.

Although the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art, Pechanek nevertheless explicitly discloses that said control connections are implemented as a bus (col. 5, lines 33-39; each PE is analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate).

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that Pechanek's use of a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten

and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

Response to Arguments

21. Applicant states on page 4, first line, that claims 1 and 7 are independent. Examiner generally notes that claim 7 is dependent on independent claim 5.

22. Applicant argues from pages 4-6 that the amendments in claims 1 and 5 are supported by the description.

However, while the amendments in claims 1 and 5 do overcome a previous written description issue, the amendments in claims 1 and 5 do catalyze additional written description issues to claims 3-4 and 7-8. These additional written description issues are explained in detail in the 112 rejection section above.

23. Applicant on page 7 argues that Batten or Nickolls, alone or in combination, do not teach particular limitations of the independent claims.

However, as explained in the rejection of the independent claims, Batten as modified by Nickolls does disclose the particular limitations of the independent claims. With regard to the newly added limitation (which also catalyzes a written description rejection), Batten discloses a connection between respective ones of said plurality of clusters (Figure 12, which shows the clusters connected to each other via connections denoted by letters I-R), and Nickolls disclose of one or more pipeline registers in a

connection depending on the distance between respective ones of said plurality of clusters (col. 20, lines 11-15, discloses of pipeline registers in the paths connecting different processing elements; col. 60, lines 1-5 disclose that pipeline registers are distributed at points being dependent on the length of various wires). The teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls with the invention of Batten in order to increase the bit flow rate of the path.

24. Applicant argues on page 8 that Nickolls is not analogous art because it relates to transmission of information through so-called massively-parallel Single Instruction Multiple Data (SIMD) computing machines and not a clustered Instruction Level Parallelism processor as claimed, and that it is thus not seen how the elements of a massively-parallel Single Instruction Multiple Data (SIMD) computing machine, although similar sounding, can be used in a clustered Instruction Level Parallelism processor.

However, examiner first notes that the examiner's combination did not entail the insertion of Nickolls' elements of a massively-parallel Single Instruction Multiple Data (SIMD) computing machine into the system of Batten. Rather, the examiner's combination only entailed the use of pipeline registers into already existing connections. The use of pipeline registers to increase the bit flow of a long path is applicable regardless of the overall environment in which that path resides, and thus its usefulness is not exclusive to Nickolls overall massively-parallel SIMD computing machine.

25. Applicant argues on page 8 that "[t]o simply state that the general idea of using elements of a computer in a processor would be an obvious modification to one skilled in the art begs the question. How?"

However, examiner has explained the combination of Nickolls' pipeline registers into the invention of Batten, and has further provided a proper motivation which would motivate one of ordinary skill in the art at the time of the invention to combine the pipeline registers of Nickolls into the invention of Batten in the specific manner which correlates to the instant claims.

26. Applicant inquires on pages 8-9 as to "[w]hat reference teaches, and moreover provides the motivation to combine with the present method, an actual real world reduction to practice of such an "obvious modification to have also determined the intention of the user"? How is the integration to occur? What suggests the desirability of such a combination?"

However, examiner has provided a motivation in the rejection above. Namely, the teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Applicant does not address this motivation with specific arguments.

27. Applicant respectfully requests on page 9 that the Examiner's position be supported by a reference, as per MPEP 2144.03.

However, as noted above, the examiner had cited a reference (Nickolls) to motivate the combination used in the rejection.

28. Applicant argues on page 9 that "[f]urther, Appellants respectfully submit that the Office Action has used impermissible hindsight to reject claims under 35 U.S.C. § 103(a). The Federal Circuit in In re Rouffet stated that virtually all inventions are combinations of old elements. Therefore an Examiner may often find many elements of a claimed invention in the prior art. To prevent the use of hindsight based on the invention to defeat patentability of the invention, the Examiner is required to show a motivation to combine the references and further a motivation to modify the combination to justify a finding of obviousness. Appellants respectfully submit that the Office Action has not met this burden."

However, as previously noted, examiner has provided a motivation in the rejection above. Namely, the teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it is unclear as to why applicants submit that the Office Action has not met this burden.

29. Applicant argues on page 9 that "[t]he mere fact that the prior art device could be modified so as to produce the claimed device, which in this case even in combination it does not (as noted above), is not a basis for an obviousness rejection unless the prior art suggested the desirability of the modification. See, In re Gordon, 733 F.2d 900, 902 (Fed, Cir. 1984); and In re Laskowski, 871 F.2d 115, 117 (Fed. Cir. 1989). The only

suggestion that can be found anywhere for making the modification appears to come from the present patent application itself.

However, as previously noted, examiner has provided a motivation in the rejection above. Namely, the teaching of Nickolls' increases the bit flow rate of the path (Nickolls, col. 23, lines 13-16). Therefore, it is unclear as to why applicant states that the only suggestion that can be found anywhere for making the modification appears to come from the present patent application itself.

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEITH VICARY whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Keith Vicary/
Examiner, Art Unit 2183